IN THE SPECIFICATION

Please replace the paragraphs below with the amended paragraphs as follows:

BSH 11/15/07

On page 9, beginning lines 16-21:

For example, messages between the switch controller SWC-A 310_A and the primary head-end controller 130_1 may be sent bi-directionally via signal path 317_A, through the first Ethernet switch 144_1, and then through signal path 119_1. Similarly, messages between the switch controller SWC_B 310_B and the primary head-end controller $\underline{130_1}$ ~~119_1~~ may be sent bi-directionally via signal paths 317_B, through the second Ethernet switch 144_2, and then through signal $\underline{\text{path } 119_2}$ ~~paths 119_V~~. Likewise, communications between the secondary switch controller SWC-B 310_B and the secondary head-end controller 130_2 may be provided in a similar manner, as shown in FIG. 1.

B1

BSH 11/15/07

On page 11, beginning lines 15-27:

During operation, in an exemplary embodiment I/O port 1 320_1 pings I/O port 2 320_2 first, then 5 milliseconds later pings I/O port 3 320_3, then 5 milliseconds later pings I/O port 4 320_4, and continues in this manner through I/O port 16 320_{16} before repeating the cycle, i.e., in a "round robin" process. [[.]] In addition, the other I/O ports 2 through 16 320_2 through 320_{16} are likewise pinging one another in a similar manner. Furthermore, a few fractions of a millisecond after each ping is sent, 16 acknowledgements are being sent from the recipient I/O port 320 back to the originating I/O port. Once an I/O port has consecutively pinged the other 15 I/O ports, a cycle has been completed. Thus, during each 5-millisecond interval, 16 individual pings and corresponding acknowledgements are being passed through the switch matrix 306_A of the primary switch controller 310_A. Therefore, during the course of one complete cycle (i.e., 75 milliseconds) the switch matrix 306_A functions as a 16x16 array, and will have transferred 240 pings and 240 acknowledgement signals.

B2

IN THE SPECIFICATION

Please replace the following paragraphs with the amended paragraphs as follows:

BSH 11/15/07

On page 12, lines 18-24:

In step 714, the secondary switch controller 310_B reads the status registers 424 of the I/O ports 320 to determine if some (e.g., at least two) or all of the I/O ports 320 have asserted an error bit in their respective status registers 424. If the determination is affirmatively answered, the [[The]] method 700 then proceeds to step 716, where the secondary switch controller 310_B assumes the primary switch controller 310_A (e.g., switch matrix 306_A) is inoperable. Thus, in step 716, the secondary switch controller 310_B will initiate a switchover and thereby serve as the primary switch controller for the switch 113.

a1

On page 14, lines 11-17:

In step 814, the secondary switch controller 310_B reads the status registers 424 of the I/O ports 320 to determine if some (e.g., at least two) or all of the I/O ports 320 have asserted an error bit in their respective status registers 424. If the determination is affirmatively answered, the [[The]] method 800 then proceeds to step 816, where the secondary switch controller 310_B assumes the primary switch controller 310_A is inoperable. Thus, in step 816, the secondary switch controller 310_B will initiate a switchover and thereby serve as the primary switch controller for the switch 113.

a2

On page 16, lines 13-19:

In the event that the switch controller [[320]] 310 fails, all of the video sessions being executed and streamed to the subscribers would be lost. Therefore, by adding a secondary switch controller 310 to the switch 113, the I/O ports 320 have an alternate switch controller available to provide an alternate in-band signal path 315 between the switch controller 310 and I/O ports 320. Accordingly, if one switch controller fails, then utilizing a redundant switch controller 310 may avert a single point of failure occurring at the switch 113.

a3